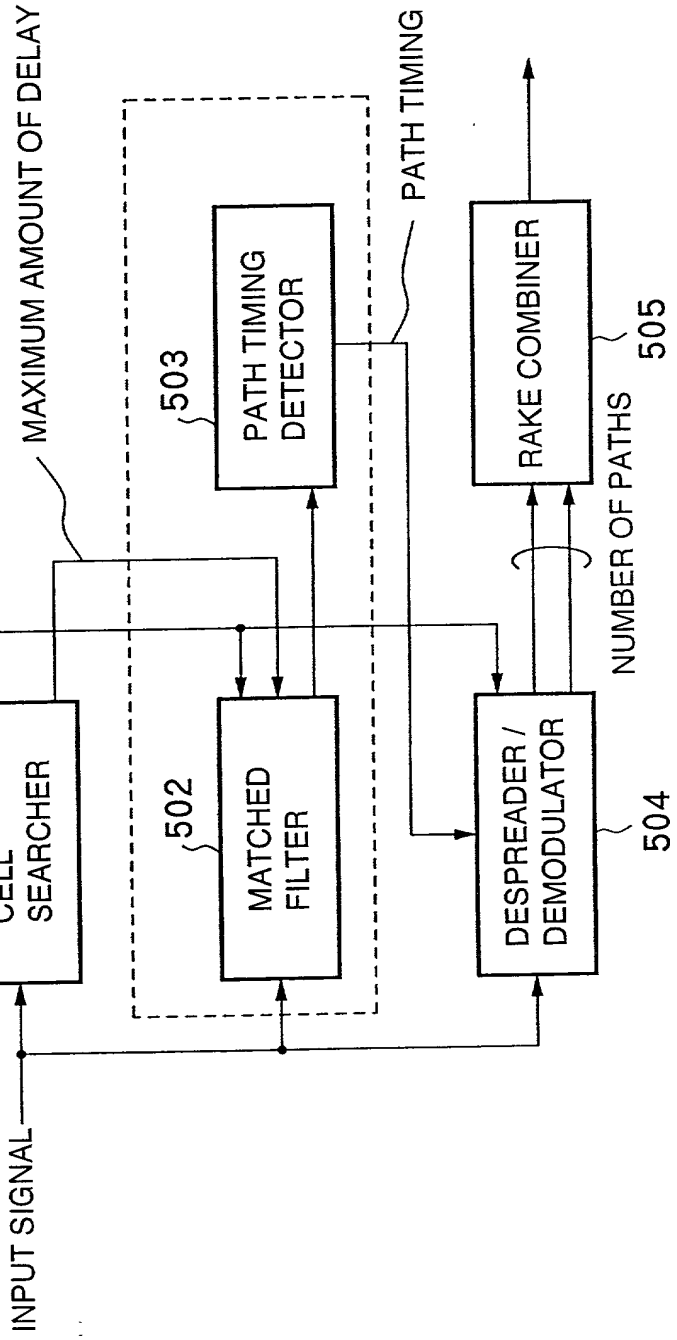
FIG. 1


INPUT SIGNAL
501
CELL SEARCHER
SYMBOL TIMING
MAXIMUM AMOUNT OF DELAY
502
MATCHED FILTER
503
PATH TIMING DETECTOR
PATH TIMING
504
DESPREADER / DEMODULATOR
NUMBER OF PATHS
505
RAKE COMBINER

# FIG. 2

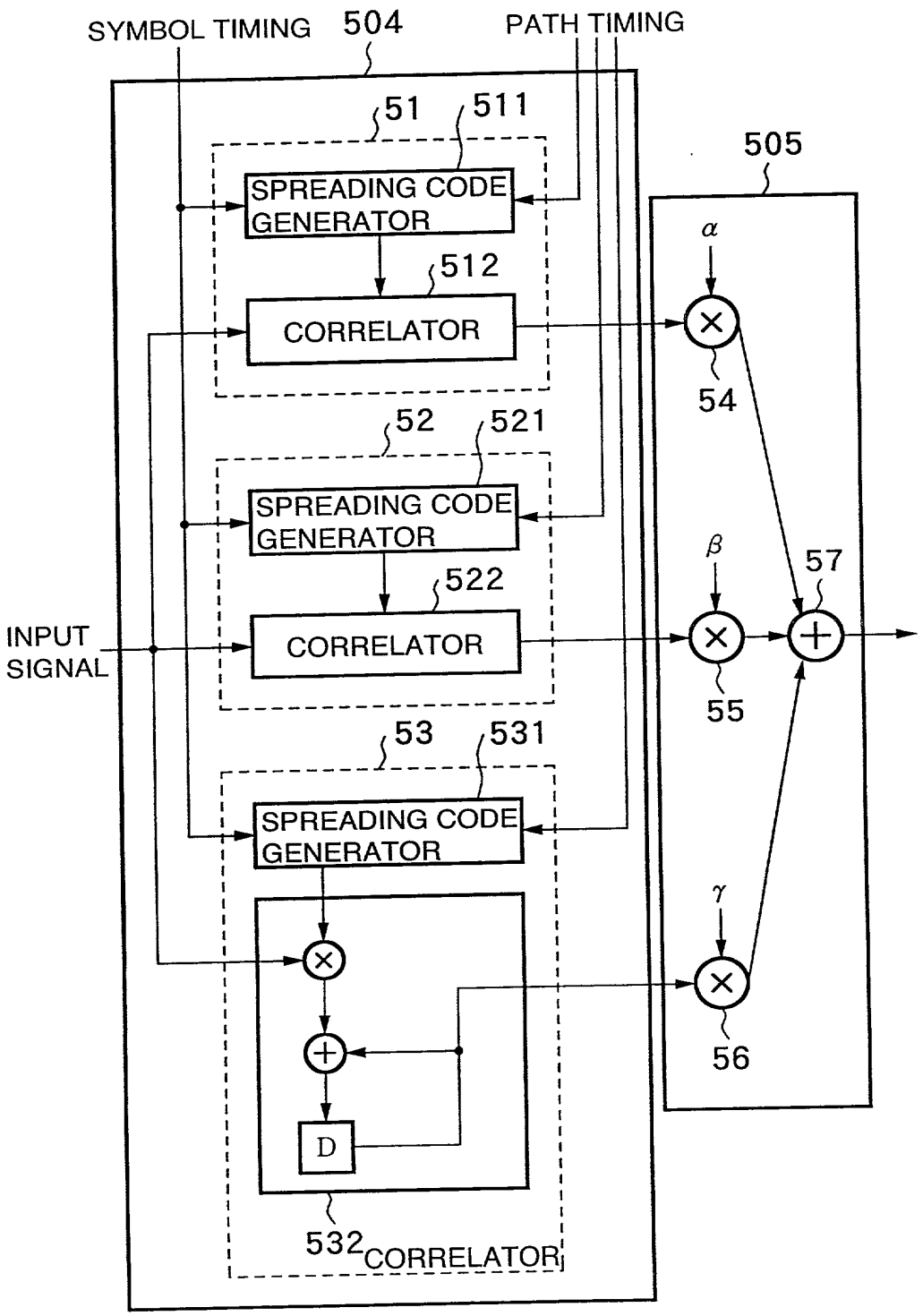

SYMBOL TIMING
504
PATH TIMING
51
511
505
SPREADING CODE GENERATOR
α
512
CORRELATOR
54
52
521
SPREADING CODE GENERATOR
β
57
522
INPUT SIGNAL
CORRELATOR
55
53
531
SPREADING CODE GENERATOR
γ
D
56
532
CORRELATOR

FIG. 3

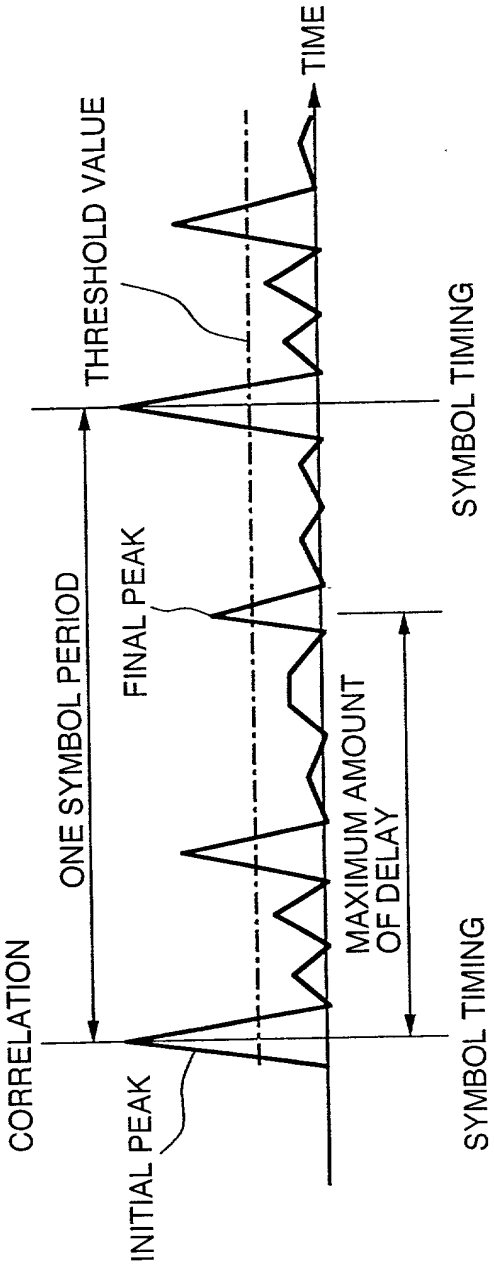

TIME
THRESHOLD VALUE
SYMBOL TIMING
ONE SYMBOL PERIOD
FINAL PEAK
MAXIMUM AMOUNT
OF DELAY
CORRELATION
INITIAL PEAK
SYMBOL TIMING

FIG. 4

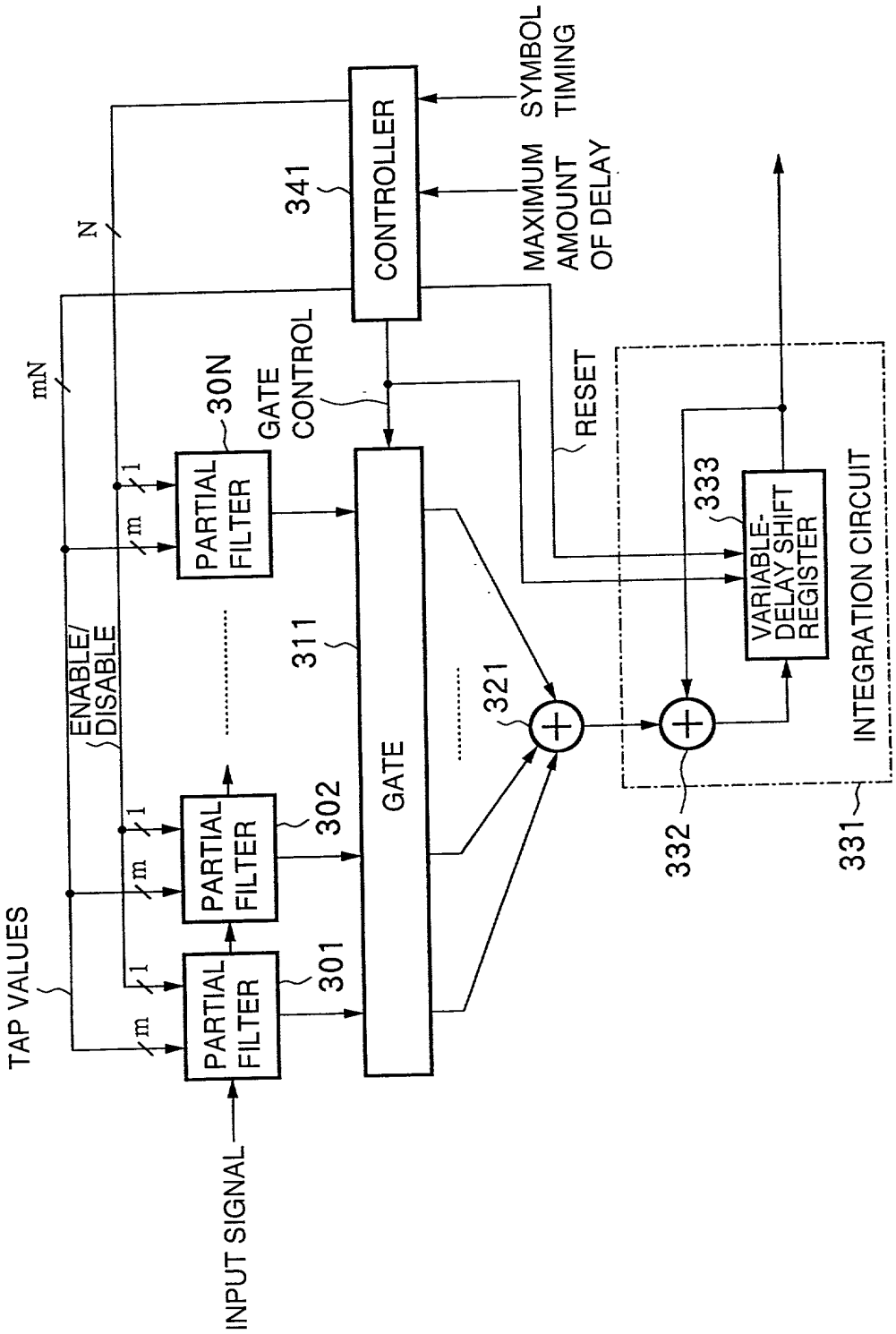

INPUT SIGNAL
TAP VALUES
ENABLE/DISABLE
PARTIAL FILTER
301
PARTIAL FILTER
302
PARTIAL FILTER
30N
GATE
311
GATE CONTROL
CONTROLLER
341
SYMBOL TIMING
MAXIMUM AMOUNT OF DELAY
RESET
321
333
VARIABLE-DELAY SHIFT REGISTER
INTEGRATION CIRCUIT
331
332
N
mN
m
1

FIG. 5

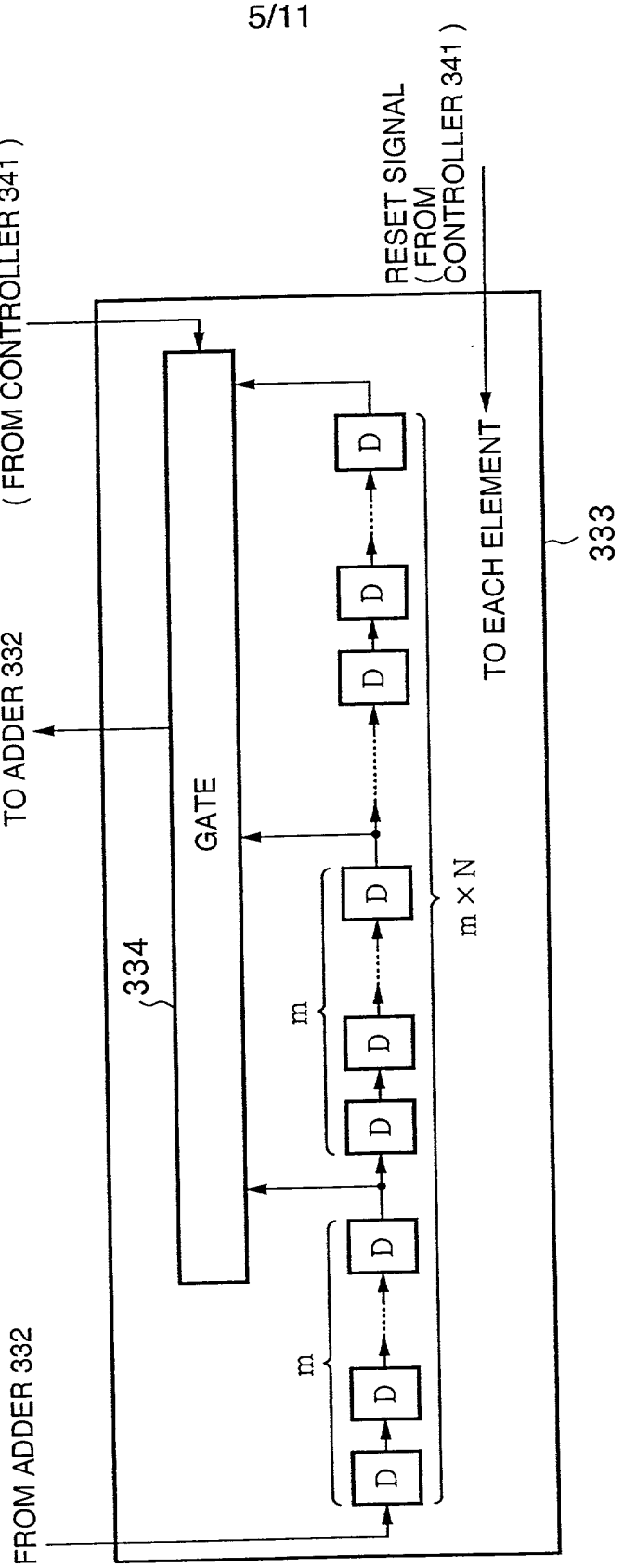
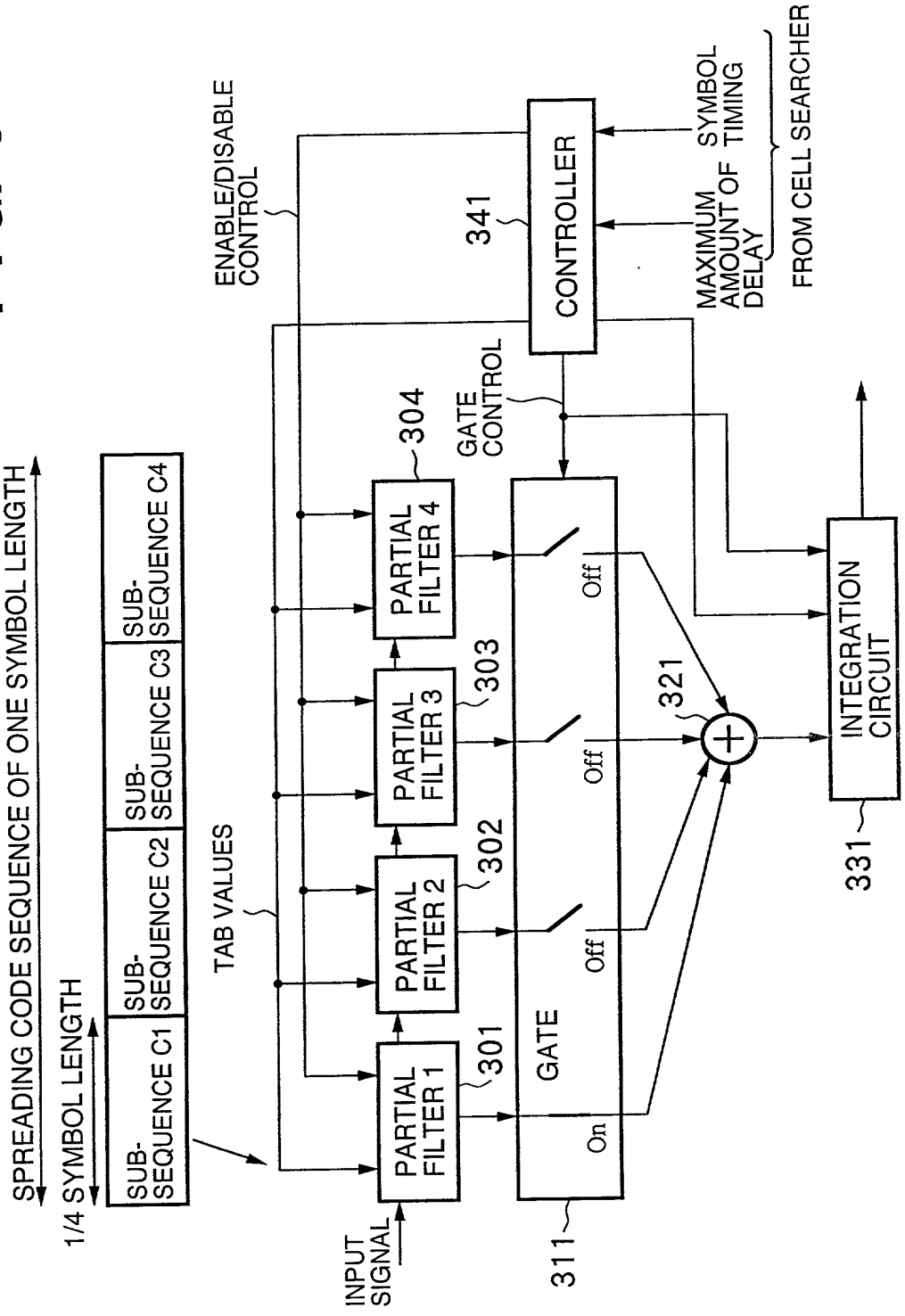

GATE CONTROL SIGNAL
(FROM CONTROLLER 341)
RESET SIGNAL
(FROM
CONTROLLER 341)
TO ADDER 332
GATE
334
TO EACH ELEMENT
333
FROM ADDER 332
D
m
m × N

FIG. 6


SPREADING CODE SEQUENCE OF ONE SYMBOL LENGTH
1/4 SYMBOL LENGTH
SUB-SEQUENCE C1
SUB-SEQUENCE C2
SUB-SEQUENCE C3
SUB-SEQUENCE C4
TAB VALUES
ENABLE/DISABLE CONTROL
341
CONTROLLER
MAXIMUM AMOUNT OF DELAY
SYMBOL TIMING
FROM CELL SEARCHER
GATE CONTROL
304
PARTIAL FILTER 4
303
PARTIAL FILTER 3
302
PARTIAL FILTER 2
301
PARTIAL FILTER 1
INPUT SIGNAL
GATE
On
Off
Off
Off
311
321
INTEGRATION CIRCUIT
331

# FIG. 7

$$Ts1: \underbrace{(c_1d_1 + c_2d_2 + c_3d_3 + c_4d_4)}_{A} + \underbrace{(c_5d_5 + c_6d_6 + c_7d_7 + c_8d_8)}_{B} + \underbrace{(c_9d_9 + c_{10}d_{10} + c_{11}d_{11} + c_{12}d_{12})}_{C} + \underbrace{(c_{13}d_{13} + c_{14}d_{14} + c_{15}d_{15} + c_{16}d_{16})}_{D}$$

$$Ts2: \underbrace{(c_1d_2 + c_2d_3 + c_3d_4 + c_4d_5)}_{E} + \underbrace{(c_5d_6 + c_6d_7 + c_7d_8 + c_8d_9)}_{F} + \underbrace{(c_9d_{10} + c_{10}d_{11} + c_{11}d_{12} + c_{12}d_{13})}_{G} + \underbrace{(c_{13}d_{14} + c_{14}d_{15} + c_{15}d_{16} + c_{16}d_{17})}_{H}$$

$$Ts3: \underbrace{(c_1d_3 + c_2d_4 + c_3d_5 + c_4d_6)}_{I} + \underbrace{(c_5d_7 + c_6d_8 + c_7d_9 + c_8d_{10})}_{J} + \underbrace{(c_9d_{11} + c_{10}d_{12} + c_{11}d_{13} + c_{12}d_{14})}_{K} + \underbrace{(c_{13}d_{15} + c_{14}d_{16} + c_{15}d_{17} + c_{16}d_{18})}_{L}$$

$$Ts4: \underbrace{(c_1d_4 + c_2d_5 + c_3d_6 + c_4d_7)}_{M} + \underbrace{(c_5d_8 + c_6d_9 + c_7d_{10} + c_8d_{11})}_{N} + \underbrace{(c_9d_{12} + c_{10}d_{13} + c_{11}d_{14} + c_{12}d_{15})}_{O} + \underbrace{(c_{13}d_{16} + c_{14}d_{17} + c_{15}d_{18} + c_{16}d_{19})}_{P}$$

$$\vdots$$

$$Ts16: c_1d_{16}+c_2d_{17}+c_3d_{18}+c_4d_{19}+c_5d_{20}+c_6d_{21}+c_7d_{22}+c_8d_{23}+c_9d_{24}+c_{10}d_{25}+c_{11}d_{26}+c_{12}d_{27}+c_{13}d_{28}+c_{14}d_{29}+c_{15}d_{30}+c_{16}d_{31}$$

# FIG. 8A

$C1=(c_{1,1}, c_{1,2}, c_{1,3}, c_{1,4})=(c_1, c_2, c_3, c_4)$

$C2=(c_{2,1}, c_{2,2}, c_{2,3}, c_{2,4})=(c_5, c_6, c_7, c_8)$

$C3=(c_{3,1}, c_{3,2}, c_{3,3}, c_{3,4})=(c_9, c_{10}, c_{11}, c_{12})$

$C4=(c_{4,1}, c_{4,2}, c_{4,3}, c_{4,4})=(c_{13}, c_{14}, c_{15}, c_{16})$

# FIG. 8B

Ts1: $c_1d_1+c_2d_2+c_3d_3+c_4d_4 = A$

Ts2: $c_1d_2+c_2d_3+c_3d_4+c_4d_5 = E$

Ts3: $c_1d_3+c_2d_4+c_3d_5+c_4d_6 = I$

Ts4: $c_1d_4+c_2d_5+c_3d_6+c_4d_7 = M$

Ts5: $c_5d_5+c_6d_6+c_7d_7+c_8d_8 = B$

Ts6: $c_5d_6+c_6d_7+c_7d_8+c_8d_9 = F$

Ts7: $c_5d_7+c_6d_8+c_7d_9+c_8d_{10} = J$

Ts8: $c_5d_8+c_6d_9+c_7d_{10}+c_8d_{11} = N$

Ts9: $c_9d_9+c_{10}d_{10}+c_{11}d_{11}+c_{12}d_{12} = C$

Ts10: $c_9d_{10}+c_{10}d_{11}+c_{11}d_{12}+c_{12}d_{13} = G$

Ts11: $c_9d_{11}+c_{10}d_{12}+c_{11}d_{13}+c_{12}d_{14} = K$

Ts12: $c_9d_{12}+c_{10}d_{13}+c_{11}d_{14}+c_{12}d_{15} = O$

Ts13: $c_{13}d_{13}+c_{14}d_{14}+c_{15}d_{15}+c_{16}d_{16} = D$

Ts14: $c_{13}d_{14}+c_{14}d_{15}+c_{15}d_{16}+c_{16}d_{17} = H$

Ts15: $c_{13}d_{15}+c_{14}d_{16}+c_{15}d_{17}+c_{16}d_{18} = L$

Ts16: $c_{13}d_{16}+c_{14}d_{17}+c_{15}d_{18}+c_{16}d_{19} = P$

FIG. 9

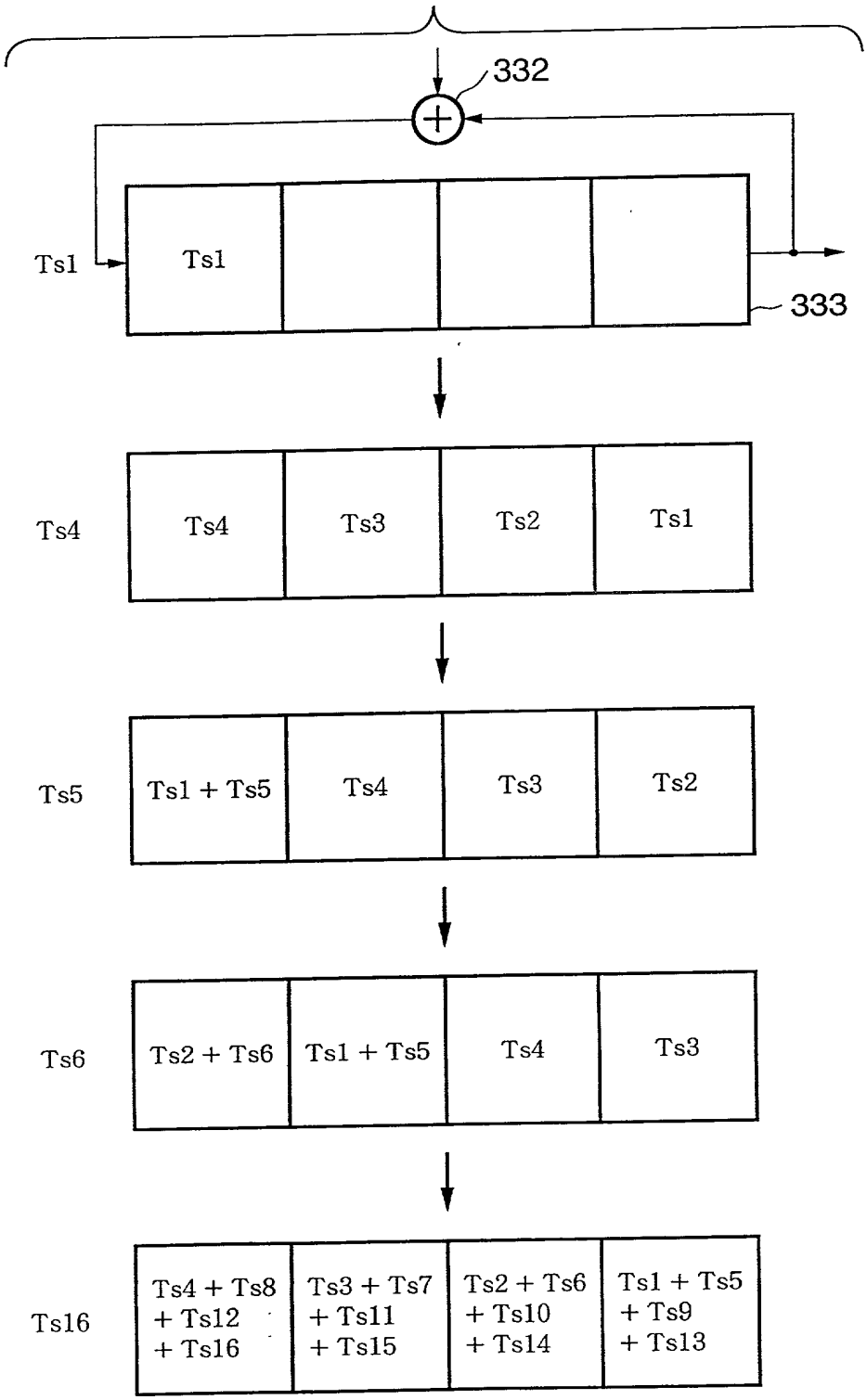

332
Ts1
Ts1
333
Ts4
Ts4
Ts3
Ts2
Ts1
Ts5
Ts1 + Ts5
Ts4
Ts3
Ts2
Ts6
Ts2 + Ts6
Ts1 + Ts5
Ts4
Ts3
Ts16
Ts4 + Ts8 + Ts12 + Ts16
Ts3 + Ts7 + Ts11 + Ts15
Ts2 + Ts6 + Ts10 + Ts14
Ts1 + Ts5 + Ts9 + Ts13

FIG. 10

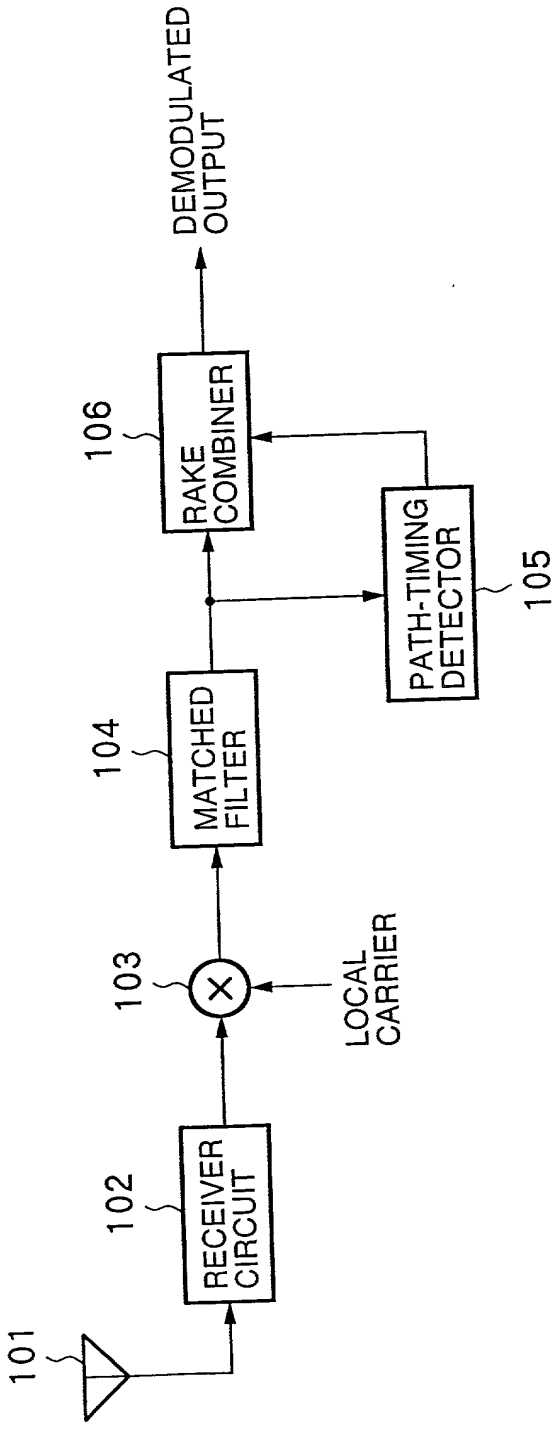
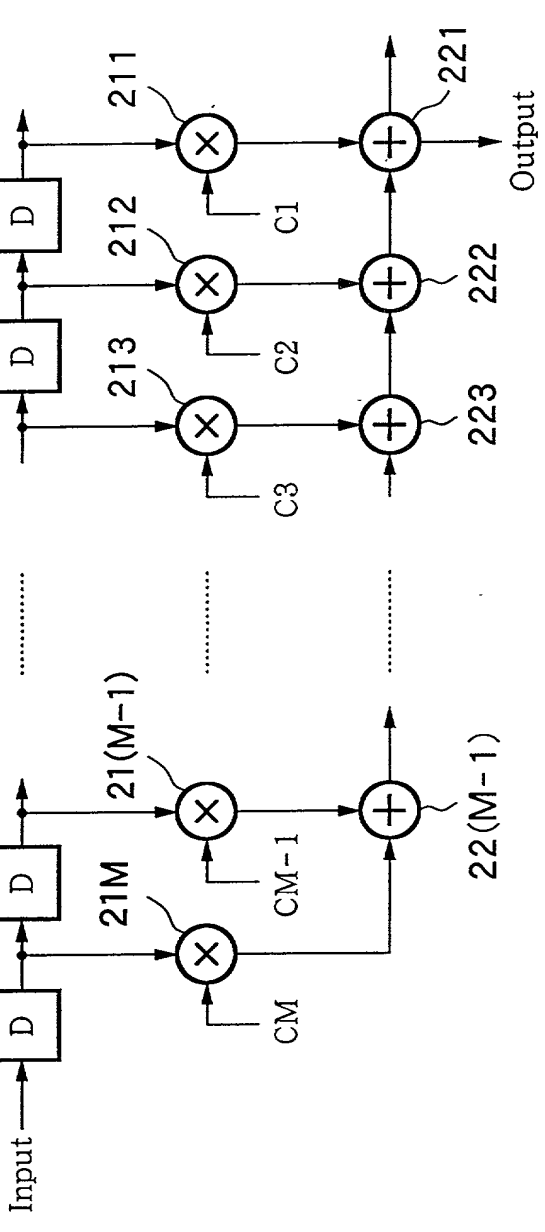

101
102
RECEIVER CIRCUIT
103
LOCAL CARRIER
104
MATCHED FILTER
105
PATH-TIMING DETECTOR
106
RAKE COMBINER
DEMODULATED OUTPUT

FIG. 11


Input
D
20M
20(M-1)
201
202
211
212
213
21M
21(M-1)
CM
CM-1
C1
C2
C3
221
222
223
22(M-1)
Output